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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

tammy@ppglaw.com

Office Action Summary

Application No.

10/534,346

Applicant(s)

SPENCER, ANTHONY

Examiner

MAXWELL A. CLARK

Art Unit

2616

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 July 2005.
2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-47 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☐ Claim(s) _____ is/are allowed.
6) ☒ Claim(s) 1-47 is/are rejected.
7) ☐ Claim(s) _____ is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
10) ☒ The drawing(s) filed on 09 May 2005 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-8508)
Paper No(s)/Mail Date 05/09/2005
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____

DETAILED ACTION

Drawings

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

2. Claims 21 and 41 are objected to because of the following informalities: The claims are identical. Appropriate correction is required.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim 47 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. A data carrier containing program means corresponds to a signal carrier transmitting program means which is non-statutory subject matter.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 7 and 29 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification does not mention virtual queues.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 17-21 and 37-41 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 17 recites the limitation "each processor or to each processor element". There is insufficient antecedent basis for this limitation in the claim.

Claims 17 and 37 recite the limitations "said packet records". There is insufficient antecedent basis for this limitation in the claim.

Regarding claims 18, 19, 38 and 39, the scope of protection being sought by applicant is indefinite. It is unclear what is meant by applicant by the tables being the same or different. In what respect the tables the same or different is indefinite, as a small number of possible examples, different or same information, structure, number of, etc.

Regarding claims 21 and 41, the phrase "such as" renders the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-10, 17, 21-31, 41-45 and 47 are rejected under 35 U.S.C. 102(e) as being anticipated by Donis et al. (US 2002/0075882 A1).

Regarding claim 1, Donis discloses sorting incoming data packets in real time (fig. 4, ¶0036, wherein the sorter assignments corresponds to sorting incoming data packets in real time), means for assigning an exit order to said packets in real time (fig. 4, ¶0037, wherein selecting the appropriate cell, i.e. based on QoS, see ¶0036, for transmission corresponds to a means for assigning an exit order to said packets in real time, and queue means for queuing said sorted packets for output in said exit order (fig. 4, ¶0036, wherein queues 43a-43d based on QoS corresponds to a queue means for queuing said sorted packets for output in said exit order).

Regarding claim 2, Donis discloses the sorting means is responsive to information contained within a packet whereby to determine an exit order number for

that packet (¶0036 wherein the Qos of the cell is the information contained within a packet whereby to determine an exit order for that packet).

Regarding claim 3, Donis discloses sorting means is responsive to information contained in a table whereby to determine an exit order number for that packet (fig. 9, ¶0082, wherein the fields relating to the queue depth assignment correspond to the sorting means is responsive to information contained in a table whereby to determine an exit order number for that packet).

Regarding claim 4, Donis discloses the sorting means responsive to information associated with a data packet stream in which said packet is located whereby to determine an exit order number for that packet (abstract, wherein the QoS level corresponds to the information associated with the data packet stream in which said packet is located whereby to determine an exit order number for that packet).

Regarding claim 5, Donis discloses the sorting means adapted to insert sorted packets in said queue means in exit order (fig. 4, ¶0036, wherein queues 43a-43d based on QoS corresponds to sorting means adapted to insert sorted packets in said queue means in exit order).

Regarding claim 6, Donis discloses a queue means as a single queue (fig. 4, ¶0038, element 43a implemented using a separate memory corresponds to a queue means as a single queue).

Regarding claim 7, Donis discloses a plurality of virtual queues (fig. 4, ¶0038, wherein queues 43a-43d implemented on a single queue corresponds to plurality of virtual queues).

Regarding claim 8, Donis discloses a queue manager adapted to insert packets into said queue means in exit order (fig. 10, ¶0102, wherein the assigning queue depths performed by buffer controllers corresponds to a queue manager adapted to insert packets into said queue means in exit order).

Regarding claim 9, Donis discloses dropping certain packets before being output from said queue means (fig. 6, ¶0042, wherein dropping the cell at step 64 corresponds to dropping certain packets before being output from said queue means).

Regarding claim 10, Donis discloses dropping certain packets before being queued in said queue means (fig. 6, ¶0042, wherein dropping the cell at step 64 corresponds to dropping certain packets before being queued in said queue means).

Regarding claim 17, Donis discloses tables of information for sorting said packets or said packet records (fig. 9, ¶0081-¶0082, wherein the graphical user interface comprising the fields corresponding to the queue depth corresponds to tables of information for sorting said packets or said packet records), wherein said tables are stored locally to each processor or to each processor element of a parallel processor (¶0102, wherein the processor for performing or coordinating the queue depth wherein the process may be performed by a network controller or other facility corresponds to the tables stored locally to each processor or to each processor element of a parallel processor).

Regarding claim 21, Donis discloses the sorting means implements algorithms for packet scheduling in accordance with predetermined criteria, such as WFQ, DFR, congestion avoidance (eg. WRED) or other prioritization and sorting (Abstract, wherein

the buffer manager includes a sorter unit for selectively storing based on the quality of service level corresponds to other prioritization and sorting).

Regarding claim 22, Donis discloses sorting incoming data packets in real time (fig. 4, ¶0036, wherein the sorter assignments corresponds to sorting incoming data packets in real time), means for assigning an exit order to said packets in real time (fig. 4, ¶0037, wherein selecting the appropriate cell, i.e. based on QoS, see ¶0036, for transmission corresponds to a means for assigning an exit order to said packets in real time, and queue means for queuing said sorted packets for output in said exit order (fig. 4, ¶0036, wherein queues 43a-43d based on QoS corresponds to a queue means for queuing said sorted packets for output in said exit order).

Regarding claim 23, Donis discloses the sorting means is responsive to information contained within a packet whereby to determine an exit order number for that packet (¶0036 wherein the Qos of the cell is the information contained within a packet whereby to determine an exit order for that packet).

Regarding claim 24, Donis discloses that the sorting is responsive to information contained within a packet whereby to assign an exit order number for that packet (fig. 9, ¶0082, wherein the fields relating to the queue depth assignment correspond to the sorting responsive to information contained within a packet whereby to assign an exit order number for that packet).

Regarding claim 25, Donis discloses the sorting means responsive to information associated with a data packet stream in which said packet is located whereby to determine an exit order number for that packet (abstract, wherein the QoS level

corresponds to the information associated with the data packet stream in which said packet is located whereby to determine an exit order number for that packet).

Regarding claim 26, Donis discloses packets inserted into a queue means in exit order determined by the means performing the sorting (fig. 4, ¶0036, wherein queues 43a-43d based on QoS corresponds to packets inserted into a queue means in exit order determined by the means performing the sorting).

Regarding claim 27, Donis discloses inserting sorted packets into a queue means in exit order (fig. 4, ¶0036, wherein queues 43a-43d based on QoS corresponds to inserting sorted packets into a queue means in exit order) under control of a queue manager (fig. 10, ¶0102, wherein the process of assigning queue depths may be performed by buffer controllers corresponds to inserting sorted packets into a queue means in exit order under control of a queue manager).

Regarding claim 28, Donis discloses queuing performed using a single output queue ((fig. 4, ¶0038, element 43a implemented using a separate memory corresponds to queuing performed using a single output queue).

Regarding claim 29, Donis discloses plurality of queues by means of single output queue (fig. 4, ¶0038, wherein queues 43a-43d implemented on a single queue corresponds to plurality of queues, wherein merge unit 45 corresponds to means of single output queue).

Regarding claim 30, Donis discloses dropping certain packets before being output from said queue means (fig. 6, ¶0042, wherein dropping the cell at step 64 corresponds to dropping certain packets before being output from said queue means).

Regarding claim 31, Donis discloses dropping certain packets before being queued in said queue means (fig. 6, ¶0042, wherein dropping the cell at step 64 corresponds to dropping certain packets before being queued in said queue means).

Regarding claim 41, Donis discloses the sorting means implements algorithms for packet scheduling in accordance with predetermined criteria, such as WFQ, DFR, congestion avoidance (eg. WRED) or other prioritization and sorting (Abstract, wherein the buffer manager includes a sorter unit for selectively storing based on the quality of service level corresponds to other prioritization and sorting).

Regarding claim 42, Donis discloses a computer system (¶0037, wherein one embodiment may be programmed on a general purpose computer corresponds to a computer system) and a data handling system (fig. 4 corresponds to a data handling system) for sorting incoming data packets in real time (fig. 4, ¶0036, wherein the sorter assignments corresponds to sorting incoming data packets in real time), means for assigning an exit order to said packets in real time (fig. 4, ¶0037, wherein selecting the appropriate cell, i.e. based on QoS, see ¶0036, for transmission corresponds to a means for assigning an exit order to said packets in real time, and queue means for queuing said sorted packets for output in said exit order (fig. 4, ¶0036, wherein queues 43a-43d based on QoS corresponds to a queue means for queuing said sorted packets for output in said exit order).

Regarding claim 43, Donis discloses a network processing system and a data handling system (fig. 4, corresponds to a network processing system and a data handling system) for sorting incoming data packets in real time (fig. 4, ¶0036, wherein

the sorter assignments corresponds to sorting incoming data packets in real time), means for assigning an exit order to said packets in real time (fig. 4, ¶0037, wherein selecting the appropriate cell, i.e. based on QoS, see ¶0036, for transmission corresponds to a means for assigning an exit order to said packets in real time, and queue means for queuing said sorted packets for output in said exit order (fig. 4, ¶0036, wherein queues 43a-43d based on QoS corresponds to a queue means for queuing said sorted packets for output in said exit order).

Regarding claim 44, Donis discloses a computer system (¶0037, wherein one embodiment may be programmed on a general purpose computer corresponds to a computer system) adapted to perform sorting incoming data packets in real time (fig. 4, ¶0036, wherein the sorter assignments corresponds to sorting incoming data packets in real time), means for assigning an exit order to said packets in real time (fig. 4, ¶0037, wherein selecting the appropriate cell, i.e. based on QoS, see ¶0036, for transmission corresponds to a means for assigning an exit order to said packets in real time, and queue means for queuing said sorted packets for output in said exit order (fig. 4, ¶0036, wherein queues 43a-43d based on QoS corresponds to a queue means for queuing said sorted packets for output in said exit order).

Regarding claim 45, Donis discloses a network processing system (fig. 4 corresponds to a network processing system) adapted to perform sorting incoming data packets in real time (fig. 4, ¶0036, wherein the sorter assignments corresponds to sorting incoming data packets in real time), means for assigning an exit order to said packets in real time (fig. 4, ¶0037, wherein selecting the appropriate cell, i.e. based on

QoS, see ¶0036, for transmission corresponds to a means for assigning an exit order to said packets in real time, and queue means for queuing said sorted packets for output in said exit order (fig. 4, ¶0036, wherein queues 43a-43d based on QoS corresponds to a queue means for queuing said sorted packets for output in said exit order).

Regarding claim 47, Donis discloses a data carrier (fig. 4 corresponds to a data carrier) containing program means (¶0037, wherein the embodiment may be programmed corresponds to a program means) adapted to perform sorting incoming data packets in real time), means for assigning an exit order to said packets in real time (fig. 4, ¶0037, wherein selecting the appropriate cell, i.e. based on QoS, see ¶0036, for transmission corresponds to a means for assigning an exit order to said packets in real time, and queue means for queuing said sorted packets for output in said exit order (fig. 4, ¶0036, wherein queues 43a-43d based on QoS corresponds to a queue means for queuing said sorted packets for output in said exit order).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

8. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 11-16, 20, 32-37, 40 and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Donis et al. (US 2002/0075882 A1) in view of Wilkinson et al. (USPN 6094715).

Regarding claim 11, Donis discloses the data portions of said packets are stored for output in accordance with an exit order determined for the corresponding packet record (fig. 4, ¶0037, wherein selecting the appropriate cell, i.e. based on QoS, see ¶0036, for transmission corresponds to a means for assigning an exit order to said packets in real time, and queue means for queuing said sorted packets for output in said exit order (fig. 4, ¶0036, wherein queues 43a-43d based on QoS corresponds to a queue means for queuing said sorted packets for output in said exit order). Donis does not expressly disclose sorting means and said queue means process only packet records containing information about said packets. Wilkinson Discloses sorting means and said queue means process only packet records containing information about said packets (col. 40, lines 28-31, wherein the PMEs having open buffers sized to accept packet headers, i.e. only packet records containing information about said packet, but not the data corresponds to sorting means and said queue means process only packet records containing information about said packets). It would have been obvious to one of ordinary skill in the art at the time on the application to include the sorting means and said queue means process wherein only packet records contain information about said

packets in Donis, as in Wilkinson, for the purpose of allowing parallel data and record information to be processed separately.

Regarding claim 12, Donis discloses said sorting means comprises a processor (¶0102, wherein a separate processor may be provided for performing or coordination the queue depth assignment). Donis does not expressly disclose sorting means comprises a parallel processor. Wilkinson discloses a sorting means comprising a parallel processor (col. 40, lines 28-31, wherein buffering the packets corresponds to sorting means via a parallel array processor, see abstract) for the purpose of providing a processor for massively parallel applications formed with low power CMOS with DRAM processing. It would have been obvious to one of ordinary skill in the art at the time of the application to include a sorting means comprising a parallel processor in Donis, as in Wilkinson, for the purpose of providing a processor for massively parallel applications formed with low power CMOS with DRAM processing.

Regarding claim 13, Wilkinson discloses the parallel processor an array processor (Abstract, wherein the parallel array processor corresponds to the parallel processor an array processor).

Regarding claim 14, Wilkinson discloses the array processor as a SIMD processor (abstract, wherein the chip has internal and external connections for SIMD corresponds to the array processor as a SIMD processor).

Regarding claim 15, Wilkinson discloses providing access for parallel processors to shared state (col. 25, lines 24-26, wherein the individual PME memory can be divided

into local and shared global areas programmatically corresponds to providing access for parallel processors to shared state).

Regarding claim 16, Wilkinson discloses a state engine to control access to shared state (col. 25, lines 26-29, wherein the specialized controls permitting task switching and retention of program state information at each of the PMEs interrupt execution levels correspond to state engine to control access to shared state).

Regarding claims 20, Donis discloses the process of assigning queue depths may be performed by buffer controllers wherein alternative embodiments include a separate processor for performing or coordinating queue depth assignment or the process may be performed by a network controller or other facility, see in particular paragraph 0102. Donis does not expressly disclose processors or processor elements share information from their respective tables, such that information held in the table for one processor is directly accessible by a different processor or the information held in the table in one processor element is accessible by other processing element(s) of the processor and processors have access to tables in other processors or processor elements have access to other processor elements in the processor, whereby processors or processor elements can perform table lookups on behalf of other processor(s) or processor elements of the processor. However, it would have been obvious to one of ordinary skill in the art at the time of the invention to disclose processors or processor elements share information from their respective tables, such that information held in the table for one processor is directly accessible by a different processor or the information held in the table in one processor element is accessible by

other processing element(s) of the processor and processors have access to tables in other processors or processor elements have access to other processor elements in the processor, whereby processors or processor elements can perform table lookups on behalf of other processor(s) or processor elements of the processor as it is well know that processors and associated information tables commonly share data therein between for the purpose of coordination between different elements in the system such as sorter, merger, ingress, egress, QoS determination, Queue depth optimizer, Fabric Interface controller, Buffer controller, network switch fabric, port interface controller, etc.

Regarding claim 32, Donis discloses the data portions of said packets are stored for output in accordance with an exit order determined for the corresponding packet record (fig. 4, ¶0037, wherein selecting the appropriate cell, i.e. based on QoS, see ¶0036, for transmission corresponds to a means for assigning an exit order to said packets in real time, and queue means for queuing said sorted packets for output in said exit order (fig. 4, ¶0036, wherein queues 43a-43d based on QoS corresponds to a queue means for queuing said sorted packets for output in said exit order). Donis does not expressly disclose sorting means and said queue means process only packet records containing information about said packets. Wilkinson Discloses sorting means and said queue means process only packet records containing information about said packets (col. 40, lines 28-31, wherein the PMEs having open buffers sized to accept packet headers, i.e. only packet records containing information about said packet, but not the data corresponds to sorting means and said queue means process only packet records containing information about said packets). It would have been obvious to one

of ordinary skill in the art at the time on the application to include the sorting means and said queue means process wherein only packet records contain information about said packets in Donis, as in Wilkinson, for the purpose of allowing parallel data and record information to be processed separately.

Regarding claim 33, Donis discloses said sorting means comprises a processor (¶0102, wherein a separate processor may be provided for performing or coordination the queue depth assignment). Donis does not expressly disclose sorting means comprises a parallel processor. Wilkinson discloses a sorting means comprising a parallel processor (col. 40, lines 28-31, wherein buffering the packets corresponds to sorting means via a parallel array processor, see abstract) for the purpose of providing a processor for massively parallel applications formed with low power CMOS with DRAM processing. It would have been obvious to one of ordinary skill in the art at the time of the application to include a sorting means comprising a parallel processor in Donis, as in Wilkinson, for the purpose of providing a processor for massively parallel applications formed with low power CMOS with DRAM processing.

Regarding claim 34, Wilkinson discloses the parallel processor an array processor (Abstract, wherein the parallel array processor corresponds to the parallel processor an array processor).

Regarding claim 35, Wilkinson discloses the array processor as a SIMD processor (abstract, wherein the chip has internal and external connections for SIMD corresponds to the array processor as a SIMD processor).

Regarding claim 36, Wilkinson discloses providing access for parallel processors to shared state (col. 25, lines 24-26, wherein the individual PME memory can be divided into local and shared global areas programmatically corresponds to providing access for parallel processors to shared state) and a state engine to control access to shared state (col. 25, lines 26-29, wherein the specialized controls permitting task switching and retention of program state information at each of the PMEs interrupt execution levels correspond to state engine to control access to shared state).

Regarding claim 37, Donis discloses tables of information for sorting said packets or said packet records (fig. 9, ¶¶0081-¶¶0082, wherein the graphical user interface comprising the fields corresponding to the queue depth corresponds to tables of information for sorting said packets or said packet records), wherein said tables are stored locally to each processor or to each processor element of a parallel processor (¶¶0102, wherein the processor for performing or coordinating the queue depth wherein the process may be performed by a network controller or other facility corresponds to the tables stored locally to each processor or to each processor element of a parallel processor).

Regarding claims 40, Donis discloses the process of assigning queue depths may be performed by buffer controllers wherein alternative embodiments include a separate processor for performing or coordinating queue depth assignment or the process may be performed by a network controller or other facility, see in particular paragraph 0102. Donis does not expressly disclose processors or processor elements share information from their respective tables, such that information held in the table for

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one processor is directly accessible by a different processor or the information held in the table in one processor element is accessible by other processing element(s) of the processor and processors have access to tables in other processors or processor elements have access to other processor elements in the processor, whereby processors or processor elements can perform table lookups on behalf of other processor(s) or processor elements of the processor. However, it would have been obvious to one of ordinary skill in the art at the time of the invention to disclose processors or processor elements share information from their respective tables, such that information held in the table for one processor is directly accessible by a different processor or the information held in the table in one processor element is accessible by other processing element(s) of the processor and processors have access to tables in other processors or processor elements have access to other processor elements in the processor, whereby processors or processor elements can perform table lookups on behalf of other processor(s) or processor elements of the processor as it is well known that processors and associated information tables commonly share data therein between for the purpose of coordination between different elements in the system such as sorter, merger, ingress, egress, QoS determination, Queue depth optimizer, Fabric Interface controller, Buffer controller, network switch fabric, port interface controller, etc.

Regarding claim 46, examiner takes official notice that at the time of the application a computer system for sorting data packets is implemented as one or more silicon integrated circuits.

Claims 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Donis et al. (US 2002/0075882 A1) in view of Matsuo et al. (US 2003/0227925).

Regarding claim 18, Donis discloses tables of information for sorting said packets or said packet records (fig. 9, ¶¶0081-¶¶0082, wherein the graphical user interface comprising the fields corresponding to the queue depth corresponds to tables of information for sorting said packets or said packet records), wherein said tables are stored locally to each processor or to each processor element of a parallel processor (¶¶0102, wherein the processor for performing or coordinating the queue depth wherein the process may be performed by a network controller or other facility corresponds to the tables stored locally to each processor or to each processor element of a parallel processor). Donis does not expressly disclose tables are the same on each processor or on each processor element of a parallel processor. Matsuo discloses tables are the same on each processor or on each processor element of a parallel processor (¶¶0065, wherein the same number of information transfer/receipt tables as the number of processors in charge of the pre-search process corresponds to the table are the same on each processor or on each processor element of a parallel processor) for the purpose of enabling the writing of necessary items of information such as head address of a packet data storage location in the packet buffer module, header information serving as a basis of search data and so forth. It would have been obvious to one of ordinary skill in the art at the time of the application to include tables that are the same on each processor or on each processor element of a parallel processor in Donis, as in Matsuo, for the purpose of enabling the writing of necessary items of information such

as head address of a packet data storage location in the packet buffer module, header information serving as a basis of search data and so forth.

Regarding claim 19, Donis discloses tables of information for sorting said packets or said packet records (fig. 9, ¶0081-¶0082, wherein the graphical user interface comprising the fields corresponding to the queue depth corresponds to tables of information for sorting said packets or said packet records), wherein said tables are stored locally to each processor or to each processor element of a parallel processor (¶0102, wherein the processor for performing or coordinating the queue depth wherein the process may be performed by a network controller or other facility corresponds to the tables stored locally to each processor or to each processor element of a parallel processor). Donis does not expressly disclose tables are different on different processors or on different processor elements of a parallel processor. Matsuo discloses a statistics request table (¶0163, wherein the statistics request table corresponds to tables that are different on different processors or on different processor elements of a parallel processor), which is different from the transfer / receipt table, for the purpose of gathering the next queues statistics. It would have been obvious to one of ordinary skill in the art at the time of the application to include a statistics request table in Donis, as in Matsuo, for the purpose of gathering the next queues statistics.

Claims 38-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Donis et al. (US 2002/0075882 A1) in view of Wilkinson et al. (USPN 6094715) further in view of Matsuo et al. (US 2003/0227925).

Regarding claim 38, Donis discloses tables of information for sorting said packets or said packet records (fig. 9, ¶0081-¶0082, wherein the graphical user interface comprising the fields corresponding to the queue depth corresponds to tables of information for sorting said packets or said packet records), wherein said tables are stored locally to each processor or to each processor element of a parallel processor (¶0102, wherein the processor for performing or coordinating the queue depth wherein the process may be performed by a network controller or other facility corresponds to the tables stored locally to each processor or to each processor element of a parallel processor). Wilkinson discloses providing access for parallel processors to shared state (col. 25, lines 24-26, wherein the individual PME memory can be divided into local and shared global areas programmatically corresponds to providing access for parallel processors to shared state) and a state engine to control access to shared state (col. 25, lines 26-29, wherein the specialized controls permitting task switching and retention of program state information at each of the PMEs interrupt execution levels correspond to state engine to control access to shared state). Donis does not expressly disclose tables are the same on each processor or on each processor element of a parallel processor. Wilkinson does not expressly disclose does not expressly disclose tables are the same on each processor or on each processor element of a parallel processor. Matsuo discloses tables are the same on each processor or on each processor element of a parallel processor (¶0065, wherein the same number of information transfer/receipt tables as the number of processors in charge of the pre-search process corresponds to the table are the same on each processor or on each processor element of a parallel

processor) for the purpose of enabling the writing of necessary items of information such as head address of a packet data storage location in the packet buffer module, header information serving as a basis of search data and so forth. It would have been obvious to one of ordinary skill in the art at the time of the application to include tables that are the same on each processor or on each processor element of a parallel processor in Donis or Wilkinson, as in Matsuo, for the purpose of enabling the writing of necessary items of information such as head address of a packet data storage location in the packet buffer module, header information serving as a basis of search data and so forth.

Regarding claim 39, Donis discloses tables of information for sorting said packets or said packet records (fig. 9, ¶¶0081-¶0082, wherein the graphical user interface comprising the fields corresponding to the queue depth corresponds to tables of information for sorting said packets or said packet records), wherein said tables are stored locally to each processor or to each processor element of a parallel processor (¶0102, wherein the processor for performing or coordinating the queue depth wherein the process may be performed by a network controller or other facility corresponds to the tables stored locally to each processor or to each processor element of a parallel processor). Wilkinson discloses providing access for parallel processors to shared state (col. 25, lines 24-26, wherein the individual PME memory can be divided into local and shared global areas programmatically corresponds to providing access for parallel processors to shared state) and a state engine to control access to shared state (col. 25, lines 26-29, wherein the specialized controls permitting task switching and retention

of program state information at each of the PME's interrupt execution levels correspond to state engine to control access to shared state). Donis does not expressly disclose tables are different on different processors or on different processor elements of a parallel processor. Wilkinson does not expressly disclose tables are different on different processors or on different processor elements of a parallel processor. Matsuo discloses a statistics request table (¶0163, wherein the statistics request table corresponds to tables that are different on different processors or on different processor elements of a parallel processor), which is different from the transfer / receipt table, for the purpose of gathering the next queues statistics. It would have been obvious to one of ordinary skill in the art at the time of the application to include a statistics request table in Donis or Wilkinson, as in Matsuo, for the purpose of gathering the next queues statistics.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Craig, Robert George Alexander et al. (US 20010024446 A1), Lee; Barry et al. (US 6996117 B2), Bass; Brian M. et al. (US 6052375 A), Short; Phillip (US 5633865 A).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MAXWELL A. CLARK whose telephone number is (571) 270-1956. The examiner can normally be reached on Monday through Thursday 7:30A.M. To 5P.M. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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June 30, 2008

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